Remarks

Claims 3, 4, 6, 9, 10, 12, 22, and 23 are presently active.

In the office action dated 24 January 2003 ("Office Action"), claims 3, 4, 6, 9, 10, 12, 22, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable by Sudo et al., U.S. patent 5,812,018 ("Sudo") in view of Chang, U.S. patent 6,396,326 ("Chang"); and claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art, Figs. 1-4 in the present application, in view of Nakano, U.S. patent 5,917,366 (Nakano) and further in view of Chang.

Applicants acknowledge with appreciation the phone conference with Examiner Nguyen on 20 March 2003. During that interview, it was discussed that Applicants would amend the claims so that it is clear that the invention provides the maximum (or minimum) of an input signal. Further discussion of this is given below.

35 U.S.C. §103(a) rejection of claims 3, 4, 6, 9, 10, 12, 22, and 23 over Sudo and Chang

Claim 3 is amended to recite that the output voltage is indicative of a local time-average maximum of the input signal voltage. This limitation is neither taught nor suggested by Sudo and Chang, whether taken separately or in combination, as discussed below.

Sudo teaches a voltage booster. Referring to Fig. 1 of Sudo, a voltage booster is taught where a voltage V_{PP} higher than V_{CC} is provided at node N15 when transistor 1 is ON and transistor 2 is OFF, and a voltage V_{BB} lower than ground (GND) is provided at node N10 when transistor 1 is OFF and transistor 2 is ON. Consider the case in which the voltage booster is in the mode to provide V_{PP} (transistor 1 is ON and transistor 2 is OFF). Charge is transferred from left to right in the circuit of Fig. 1, as indicated by the arrow for CURRENT FLOW in Fig. 1. With clock signals CLK1 and CLK2 in antiphase with respect to each other, charge is transferred from node to node in a left to right fashion, so that the voltage at a node is equal to the sum of the preceding node voltage and the transistor threshold voltage. There is seen to be a stepwise increase in node voltage from left to right, where the step size is a transistor threshold voltage. (See last paragraph of column 1 of Sudo.) Thus, the voltage at any node in Fig. 1 of Sudo does not follow the maximum of an input signal voltage. A similar discussion applies to the case in which the

voltage booster is in the mode to provide V_{BB} (transistor 1 is OFF and transistor 2is ON), where now there is a stepwise decrease in node voltage from right to left with the step size being a transistor threshold voltage.

Chang is cited in the Office Action for teaching transistors with leakage currents in excess of 1 microampere per micron of device width. Applicants respectfully disagree that Chang teaches such a feature, because leakage current in excess of 1 microampere per micron of device width occurs for transistors fabricated with sub 0.13 CMOS process technology. Such process technology has only recently become commercially available. Nevertheless, Chang certainly does not teach a circuit for providing the local time-average maximum of an input signal.

Therefore, for the above reasons, the combination of Sudo and Chang do not teach a circuit to provide a local time-average maximum of an input signal.

Claim 4 already recited the step of sampling the output voltage at the output port to provide a local time-average maximum of the input signal voltage, and therefore it also is believed non-obvious over Sudo and Chang.

Claim 6 is amended to recite that DC offset correction voltage is a local time-average maximum of the input signal voltage. Again, for the same reasons as given with respect to claim 3, claim 6 is believed patentable over Sudo and Chang.

Claim 9 is amended to recite that the output voltage is a local time-average minimum of the input signal voltage, and claim 12 is amended to recite that the DC offset correction voltage is a local time-average minimum of the input signal voltage. For the similar reasons as given above for claims 3 and 6, respectively, claims 9 and 12 are believed patentable over Sudo and Chang. Claim 10 already recited the step of sampling the output voltage at the output port to provide a local time-average minimum of the input signal voltage, so that for similar reasons, it too is believed patentable over Sudo and Chang.

Claims 22 and 23 are dependent upon claims 3 and 9, respectively, and therefore are believed patentable over Sudo and Chang.

35 U.S.C. §103(a) rejection of claims 6 and 12 over the admitted prior art (Figs. 1-4), Nakano, and Chang.

As stated in the Office Action, page 4, the admitted prior art, Figs. 1-4 of the present application, does not show a field effect transistor connected as recited in claims 6 and 12. Substituting a FET for a diode (for which Nakano is cited) in the prior art still does not lead to the claimed invention because the local time-average maximum (claim 6) or minimum (claim 12) will not be obtained unless the leakage current is sufficiently high. As discussed in the specification (see for example paragraph [0018]), a "leaky" FET allows for the tracking of the maximum or minimum, depending upon how the FET is configured. The present invention teaches, and the claims recite, that this leakage current should be in excess of 1 microampere per micron of device width. As discussed above, Chang neither teaches nor suggests transistors with leakage current in excess of 1 microampere per micron of device width. Therefore, Applicants believe that the admitted prior art, Nakano, and Chang, when taken in combination, do no suggest all limitations of claims 6 and 12.

Respectfully submitted,

Seth Z. Kalson Dated: 3-24-03

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicants and Intel Corporation (Assignee)